

Claims:

1 1. A random number generator, comprising an electrical circuit that has an unstable
2 state and a stable state which it settles into after a random period of time; a counter that
3 determines the time that it takes for the electrical circuit to settle into the stable state; and a
4 generator that generates a random number using the settle time as the random seed.

1 2. The generator of Claim 1, wherein the electrical circuit starts in the unstable state
2 when power is applied to the electrical circuit.

1 3. The generator of Claim 1, wherein the electrical circuit is forced into the unstable
2 state during the operation of the electrical circuit in order to generate a new random seed.

1 4. The generator of Claim 2, wherein the electrical circuit comprises a phase locked
2 loop.

1 5. The generator of Claim 4, wherein the counter further comprises a counter that
2 counts the number of meta-stable clock ticks of the phase locked loop during the settle time of
3 the phase locked loop and wherein the random seed comprises the number of meta-stable clock
4 ticks of the phase locked loop during the settle time.

1 6. A random number generation method, comprising:
2 providing an electrical circuit that has an unstable state and a stable state which it settles
3 into after a random period of time;
4 counting the time that it takes for the electrical circuit to settle into the stable state; and
5 generating a random seed based on the settle time of the electrical circuit.

1 7. The method of Claim 6 further comprising applying power to the electrical circuit
2 so that the electrical circuit starts in the unstable state when power is applied to the electrical
3 circuit.

1 8. The method of Claim 6 further comprising causing the electrical circuit to be
2 placed into the unstable state during the operation of the electrical circuit in order to generate a
3 new random seed.

1 9. A random seed generator, comprising:
2 an electrical circuit that has an unstable state and a stable state which it settles into after a
3 random period of time; and
4 a counter that determines the time that it takes for the electrical circuit to settle into the
5 stable state wherein the settle time corresponds to a random seed for generating a random
6 number.

1 10. The generator of Claim 9, wherein the electrical circuit starts in the unstable state
2 when power is applied to the electrical circuit.

1 11. The generator of Claim 9, wherein the electrical circuit is forced into the unstable
2 state during the operation of the electrical circuit in order to generate a new random seed.

1 12. The generator of Claim 10, wherein the electrical circuit comprises a phase locked
2 loop.

1 13. The generator of Claim 12, wherein the counter further comprises a counter that
2 counts the number of meta-stable clock ticks of the phase locked loop during the settle time of
3 the phase locked loop and wherein the random seed comprises the number of meta-stable clock
4 ticks of the phase locked loop during the settle time.

1 14. A random seed generation method, comprising:
2 providing an electrical circuit that has an unstable state and a stable state which it settles
3 into after a random period of time; and

4 counting the random time that it takes for the electrical circuit to settle into the stable state
5 wherein the settle time corresponds to a random seed for generating a random number.

1 15. The method of Claim 14 further comprising applying power to the electrical
2 circuit to put the electrical circuit into the unstable state.

1 16. The method of Claim 14 further comprising causing the electrical circuit to enter
2 the unstable state during the operation of the electrical circuit in order to generate a new random
3 seed.

1 17. A computer system that generates a random number, comprising:
2 a phase locked loop circuit that has an unstable state and a stable state that it enters after
3 some random period of time;
4 a counter for determining the period of time for the phase locked loop to settle into the
5 stable state, the settle time corresponding to a random seed; and
6 a generator for applying the random seed to a random number generator in order to
7 generate a random number.

1 18. The computer system of Claim 17, wherein the counter further comprises a
2 counter that counts the number of meta-stable clock ticks of the phase locked loop during the
3 settle time of the phase locked loop and wherein the random seed comprises the number of meta-
4 stable clock ticks of the phase locked loop during the settle time.